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TITLE: DEBUG DEVICE

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ABSTRACT:

PURPOSE: To avoid the generation of a useless break operation and to improve the debug efficiency by performing the break operation only in case the data of the prescribed value is written to a specific address of a memory of an actual device computer system.

CONSTITUTION: A data bus 12, an address bus 13 and a control bus 14 are connected to a processor 11 of an actual device computer 10. Then a multiplexer 3, a comparator 5 and a break point control circuit 7 of a debug device 1 are connected to the buses 12∼14, respectively. An AND gate 8 is

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connected to the output side of the multiplexer 3 via a bit map memory 4, and at the same time the memory writing signal sent from the bus 14 and the output of the comparator 5 are applied to the gate 8. The break point detection signal sent from the gate 8 is applied to the circuit 7 and a processor 2. Then a break operation is performed by the circuit 7 only when the data of the prescribed value is written to a specific address of the memory 4. Thus a useless break operation is prevented to improve the debug efficiency.